REMARKS

By this Amendment, Applicants propose to amend claims 1, 3, and 8. Upon entry of this Amendment, claims 1-16 remain pending.

In the Office Action of July 7, 2004[1] ("OA"), claims 1-16 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,805,861 to *Gilbert et al.* ("*Gilbert*"). Applicants address the rejection below.

Applicants traverse the rejection of claims 1-16 because *Gilbert* does not anticipate these claims. In order to properly anticipate Applicants' claimed invention under 35 U.S.C. § 102(b), each and every element of the claim at issue must be found, either expressly described or under principles of inherency, in a single prior art reference. Further, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim[s]." *See* M.P.E.P. § 2131. Finally, "[t]he elements must be arranged as required by the claim." *Id.*

Independent claim 1 recites a combination of elements including:

> a logic verification unit configured to perform a logic verification by inputting a plurality of test vectors to a circuit description defining a structure and a specification of a circuit to be designed . . .
>
> a profile information generating unit configured to store information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification in every test vector as profile information . . . and
>
> a test vector classifying unit configured to classify the test vectors into test vectors related to the changed logic cones and test vectors unrelated to the changed logic cones using the profile information.

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether or not any such statement is identified herein, Applicants decline to automatically subscribe to any statement or characterization in the Office Action.

Gilbert fails to teach or suggest at least the claimed "logic verification unit." *Gilbert* is directed to "maintaining consistency of logical component and net names used in EDA [electronic design automation] synthesis and logic optimizing tools during the . . . design process" (col. 1, lines 8-13). The Examiner alleges (OA at 2) that *Gilbert* anticipates the claimed "logic verification unit" because it discloses reading "new and old" design versions (Fig. 4, items 42-44; col. 9, lines 63-65), comparing a new cone of logic to an old cone of logic (Fig. 4, item 50), and, based on that comparison, transferring and assigning "component and net names" from the old version to the new version (Fig. 4, items 54, 58, 60). According to the Examiner, the "component and net names" disclosed by *Gilbert* are consistent with "test vectors." Applicants disagree with the Examiner's characterization of *Gilbert*.

Contrary to the Examiner's position, *Gilbert*'s "component and net names" do not constitute the claimed "test vectors." As *Gilbert* explains, component and net names refer to names of gate level objects and their connections given by a logic design synthesis tool (col. 7, lines 14-16; col. 7, line 66 – col. 8, line 2). The claimed "test vectors," in contrast, are used to perform a logic verification. For at least this reason, *Gilbert* does not teach or suggest the claimed "logic verification unit," even if *Gilbert*'s "Cone Graph Compare" process (col. 9, lines 58-59; Fig. 4) were to involve "logic verification."

Gilbert also fails to teach or suggest the claimed "profile information generating unit" and the claimed "test vector classifying unit." Despite the Examiner's allegations, "names" do not constitute the claimed "test vectors."

Because *Gilbert* does not teach or suggest each and every feature of claim 1, as a matter of law, it cannot anticipate this claim. As such, the rejection of claim 1 under 35 U.S.C. §102(b) based on *Gilbert* should be withdrawn.

Independent claims 3 and 8, although of different scope, include features similar to those of claim 1 discussed above. In particular, claim 3 recites, *inter alia*:

> performing a logic verification by inputting a plurality of test vectors to a circuit description defining a structure and a specification of a circuit to be designed . . .
>
> storing information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification in every test vector as profile information . . . and
>
> classifying the test vectors into test vectors related to the changed logic cones and test vectors unrelated to the changed logic cones using the profile information.

Likewise, claim 8 recites, *inter alia*:

> instructions configured to perform a logic verification by inputting a plurality of test vectors into a circuit description defining a structure and a specification of a circuit to be designed . . .
>
> instructions configured to store information about a plurality of logic cones in the circuit description to be activated by the test vectors during the logic verification in every test vector as profile information . . . and
>
> instructions configured to classify the test vectors into test vectors related to logic cones the changed and test vectors unrelated to the changed logic cones using the profile information.

For at least reasons similar to those presented above in connection with claim 1, independent claims 3 and 8 are not anticipated by *Gilbert*.

Because independent claims 1, 3, and 8 are not anticipated by *Gilbert*, the rejection of these claims under 35 U.S.C. § 102(b) based on *Gilbert* should be withdrawn. The rejection of claims 2, 4-7 and 9-16 should be withdrawn as well, at least because of the respective dependence of those claims from base claims 1, 3, and 8. Applicants thus request withdrawal of the rejection of claims 9-16 under 35 U.S.C. § 102(b) and the timely allowance of these pending claims.

Conclusion

Applicants request that this Amendment After Final be entered by the Examiner. The proposed amendments of claims 1, 3, and 8 do not raise new issues or necessitate the undertaking of any additional search of the art by the Examiner. This Amendment should therefore allow for immediate action by the Examiner.

Applicants point out that the final action by the Examiner presented some new arguments as to the application of the art against Applicants' invention. Entry of this Amendment would allow Applicants to reply to the final rejections and place the application in condition for allowance, or in better form for appeal, should the Examiner dispute the patentability of the pending claims.

The claimed invention is neither anticipated nor rendered obvious in view of the references cited against this application. Applicants request the Examiner's reconsideration of the application in view of the foregoing, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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